Electronic Version
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Claims

[c1] 1. A method of manufacturing an N-channel metal-oxide-semiconductor (NMOS) transistor with an P-type gate, comprising:
providing a substrate;
forming a gate dielectric layer over the substrate;
forming an indium doped polysilicon layer over the gate dielectric layer;
patterning the indium doped polysilicon layer and the gate dielectric layer to form a gate; and
forming an N-doped region in the substrate on each side of the gate.

[c2] 2. The method of claim 1, wherein the step of forming an indium doped polysilicon layer over the gate dielectric layer comprises performing an in-situ indium ion doping during a chemical vapor deposition operation.

[c3] 3. The method of claim 1, wherein the step of forming an indium doped polysilicon layer over the gate dielectric layer comprises:
forming an undoped polysilicon layer over the gate dielectric layer; and
implanting indium ions into the undoped polysilicon

layer.

[c4] 4. The method of claim 1, wherein after forming the indium doped polysilicon layer over the gate dielectric layer but before forming the gate further comprises forming a metal silicide layer over the indium doped polysilicon layer.

[c5] 5. The method of claim 4, wherein the step of patterning the indium doped polysilicon layer and the gate dielectric layer to form the gate further comprises patterning the metal silicide layer.

[c6] 6. The method of claim 4, wherein the metal silicide layer is formed by performing a chemical vapor deposition operation.

[c7] 7. The method of claim 4, wherein the metal silicide layer comprises a tungsten silicide layer.

[c8] 8. A method of manufacturing an N-channel metal-oxide semiconductor (NMOS) transistor with a P-type gate, comprising:
providing a substrate;
forming a gate dielectric layer over the substrate;
forming an indium doped polysilicon layer over the gate dielectric layer, wherein the indium doped polysilicon layer is formed by performing an in-situ doping chemical

vapor deposition operation using gaseous indium chloride ($InCl_3$) as a doping source;
patterning the indium doped polysilicon layer and the gate dielectric layer to form a gate; and
forming an N-doped region in the substrate on each side of the gate.

[c9] 9. The method of claim 8, wherein the step of forming an indium doped polysilicon layer over the gate dielectric layer comprises evaporating the solid indium chloride ($InCl_3$) to form indium chloride vapor before passing the indium chloride vapor into a reaction chamber for conducting the chemical vapor deposition process.

[c10] 10. The method of claim 9, wherein the step of evaporating solid indium chloride to form a gaseous vapor comprises heating the solid indium chloride to a temperature of about 280°C.

[c11] 11. The method of claim 8, wherein after forming the indium doped polysilicon layer over the gate dielectric layer but before forming the gate further comprises forming a metal silicide layer over the indium doped polysilicon layer.

[c12] 12. The method of claim 8, wherein the step of patterning the indium doped polysilicon layer and the gate di-

electric layer to form the gate further comprises patterning the metal silicide layer.

[c13] 13. The method of claim 8, wherein the metal silicide layer is formed by performing a chemical vapor deposition operation.

[c14] 14. The method of claim 8, wherein the metal silicide layer comprises a tungsten silicide layer.

[c15] 15. A method of manufacturing an N-channel metal-oxide-semiconductor (NMOS) transistor with an P-type gate, comprising:
providing a substrate;
forming a gate dielectric layer over the substrate;
forming an indium doped polysilicon layer over the gate dielectric layer;
forming a metal silicide layer over the indium doped polysilicon layer;
patterning the metal silicide layer, the indium doped polysilicon layer and the gate dielectric layer to form a gate; and
forming an N-doped region in the substrate on each side of the gate.

[c16] 16. The method of claim 15, wherein the step of forming an indium doped polysilicon layer over the gate dielectric

layer comprises performing an in-situ indium ion doping during a chemical vapor deposition operation using gaseous indium chloride ($InCl_3$) as a doping source.

[c17] 17. The method of claim 16, wherein the step of performing an in-situ indium ion doping in a chemical vapor deposition chamber comprises heating solid indium chloride to a temperature of about 280°C to form a gaseous vapor and passing the vapor to the chemical vapor deposition chamber.

[c18] 18. The method of claim 16, wherein the step of forming an indium doped polysilicon layer over the gate dielectric layer comprises:
forming an undoped polysilicon layer over the gate dielectric layer; and
implanting indium ions into the undoped polysilicon layer.

[c19] 19. The method of claim 18, wherein after implanting indium ions into the undoped polysilicon layer, further comprises performing an annealing operation and then performing a cleaning operation.

[c20] 20. The method of claim 15, wherein the metal silicide layer comprises a tungsten silicide layer.